

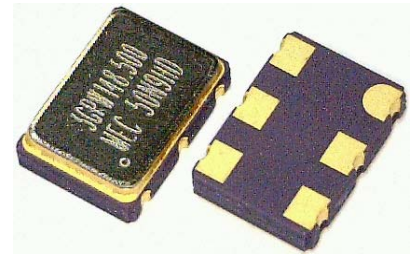
Differential LVPECL Crystal Clock Oscillators

HPK5761 Series 200 fsec Jitter +2.5V +3.3V "K" Family



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Since 1973

- ◆ Femto second integrated phase jitter (200 fs typical, 12 KHz to 20 MHz)
- ◆ Superior phase noise (-138 dBc/Hz at 10 KHz and -144 dBc/Hz at 100 KHz offset).
- ◆ High performance with surprisingly low price.
- ◆ 2.5V or 3.3V supply voltage.



General Specifications

Product Series	HPK5761; "K" family characteristics. Tri-State on pad 1							
Frequency Range	40 MHz ~ 200 MHz.							
Output Logic	Differential PECL square wave							
Frequency Stability vs Operating Temperature Range	Stability Code	Commercial "C":: -10°C to +70°C			Industrial "I":: -40°C to +85°C			
	±25 ppm	A			D			
	±50 ppm	B			E			
	±100 ppm	C			F			
	Custom ±xx ppm	Cxx			Ixx			
	If custom, use "temperature range code + desired stability in ppm" for the stability code. Example: " C20 " (±20 ppm over -10 to +70°C).							
Supply Voltage V_{CC}	+2.5 V ± 5 % (Voltage code is " 25 "); or +3.3 V ± 5 % (Voltage code is " 3 ")							
Output Voltage HIGH "1", V_{OH}	V _{DD} -1.025 V min.; V _{DD} -0.95 V typical; V _{DD} -0.88 V max. Condition: 50 ohms to V _{DD} -2V							
Output Voltage LOW "0", V_{OL}	V _{DD} -1.810 V min.; V _{DD} -1.70 V typical; V _{DD} -1.62 V max. Condition: 50 ohms to V _{DD} -2V							
Output Swing	595 mV min; 750 mV typical; 930 mV max.							
Current Consumption	35 mA typical; 50 mA max.							
Load	50 ohms into V _{CC} -2V or Thevenin equivalent (terminating resistors required on all outputs).							
Rise Time (Tr)	0.3 n sec. typ; 0.5 n sec. max. 20%→80% of waveform							
Fall Time (Tf)	0.3 n sec. typ; 0.5 n sec. max. 80%→20% of waveform							
Duty Cycle	50% ± 5% max. measured at 50% waveform							
Tri-state Function on pad No. 1	If no connection or V _{DD} *70% min is applied: Output. Internal pull-up Oscillation disable time is 0.2 u sec max.							
	If V _{DD} *30% max is applied: High impedance. Current consumption is 10 uA typical Oscillation enable time is 2 m sec. max.							
Phase Jitter (RMS)	200 fs typical (12 KHz to 20 MHz integrated)							
SSB Phase Noise (dBc/Hz). Typical	Offset	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
	125 MHz	-50	-82	-116	-138	-144	-149	-155
Start-up Time	3 ms typical; 10 m sec. max.							
Aging	±3 ppm / year max.							
Packaging	180 mm reel; 16 mm tape, 8.0 mm pitch. 1000 pcs per reel.							

⁽¹⁾Inclusive of 25°C tolerance, operating temperature range, ±10% input voltage variation, load change, aging at +25°C, shock and vibration

MERCURY www.mercury-crystal.com

Taiwan: TEL (886)-2-2406-2779, FAX (886)-2-2496-0769, e-mail: sales-tw@mercury-crystal.com

U.S.A.: TEL (1)-909-466-0427, FAX (1)-909-466-0762, e-mail: sales-us@mercury-crystal.com

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Absolute Maximum Rating Permanent damage may be created if operate beyond limits specified $T_a=25^{\circ}\text{C}$, $V_{ss}=0\text{V}$

Parameters	Rating	
	Min.	Max.
Supply Voltage	$V_{ss}-0.5\text{V}$	5.0V
Input Voltage	$V_{ss}-0.5\text{V}$	$V_{DD}+0.5\text{V}$
Output Voltage	$V_{ss}-0.5\text{V}$	$V_{DD}+0.5\text{V}$

Environmental Performance Specifications

Green Requirement	RoHS 6/6 (2002/95/EC) and WEEE (2002/96/EC) compliant
MSL Level	Level 1 per IPC/JEDEC J-STD-020D.1
Storage temp. range	-55°C to $+125^{\circ}\text{C}$
Humidity	85% RH, 85°C , 48 hours
Hermetic seal	Leak rate 2×10^{-8} ATM-cm ³ /sec max.
Solderability	MIL-STD-202F method 208E
Reflow	260°C for 10 sec max.. 2 times max.
Vibration	MIL-STD-202F method 204, 35G, 50 to 2000 Hz
Shock	MIL-STD-202F method 213B, test condi. E, 1000GG $\frac{1}{2}$ sine wave
ESD Protection	2KV max. Human body model.
Contact pad surface finish	Gold (0.3~1.0 um) on nickel (1.27~8.89 um)
Weight per unit	180 mg typical

Part Number Format and Examples:

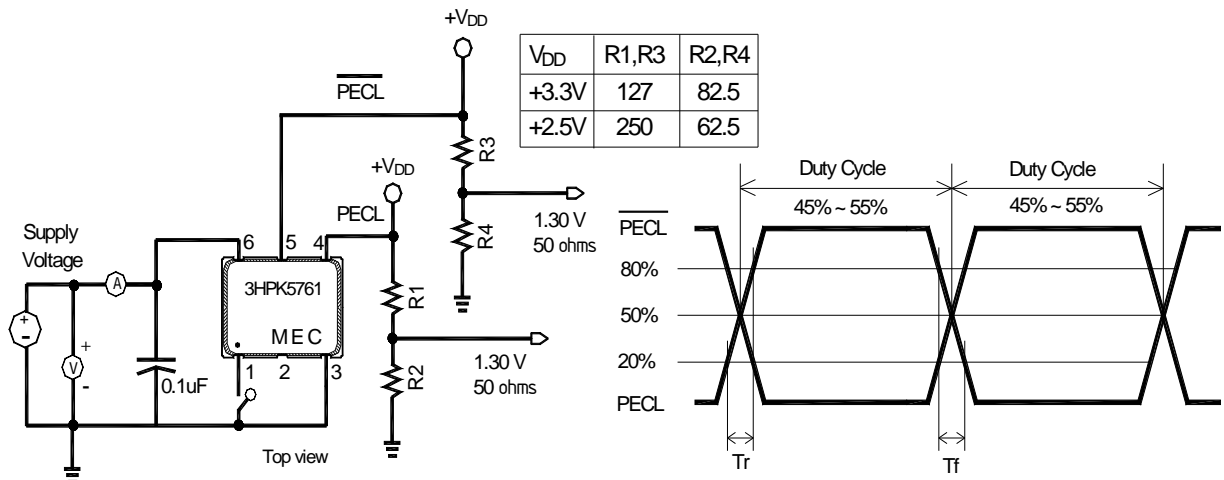
Example: 3HPK5761-A-155.520; 25HPK5761-A-155.520

Explanation: +3.3V HPK5761 series LVPECL output clock oscillator, frequency stability is ± 25 ppm over -10°C to $+70^{\circ}\text{C}$, 155.520 MHz

			⌀		⌀	⌀: customer to specify
3	HPK5761	—	A	—	155.520	
①	②		③		④	

①: V_{DD} voltage codes: "3" for +3.3 V; "25" for +2.5 V ②: HPK5761 product series. 'H' for clock; 'P' for PECL; 'K': for "K" family characteristics. "576" for 5x7 mm SMD with 6 pads. '1' for Tri-State on pad 1.
③: Frequency stability code: "A" ~ "F" or custom. See table above. ④: Frequency in MHz

25HPK5761 and 3HPK5761 Test Circuit and Waveform:



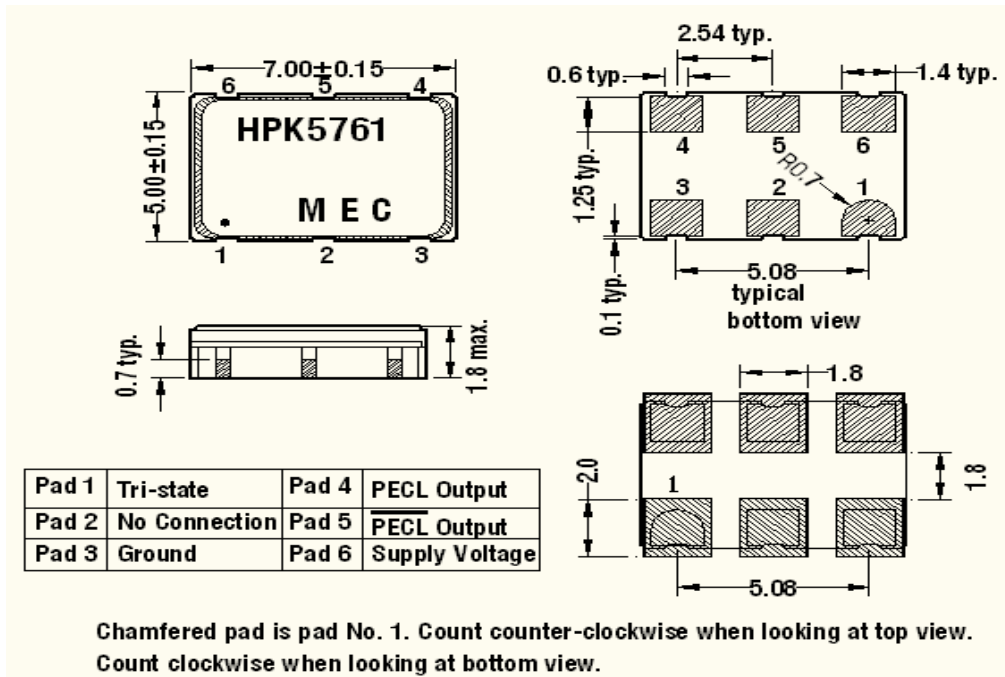
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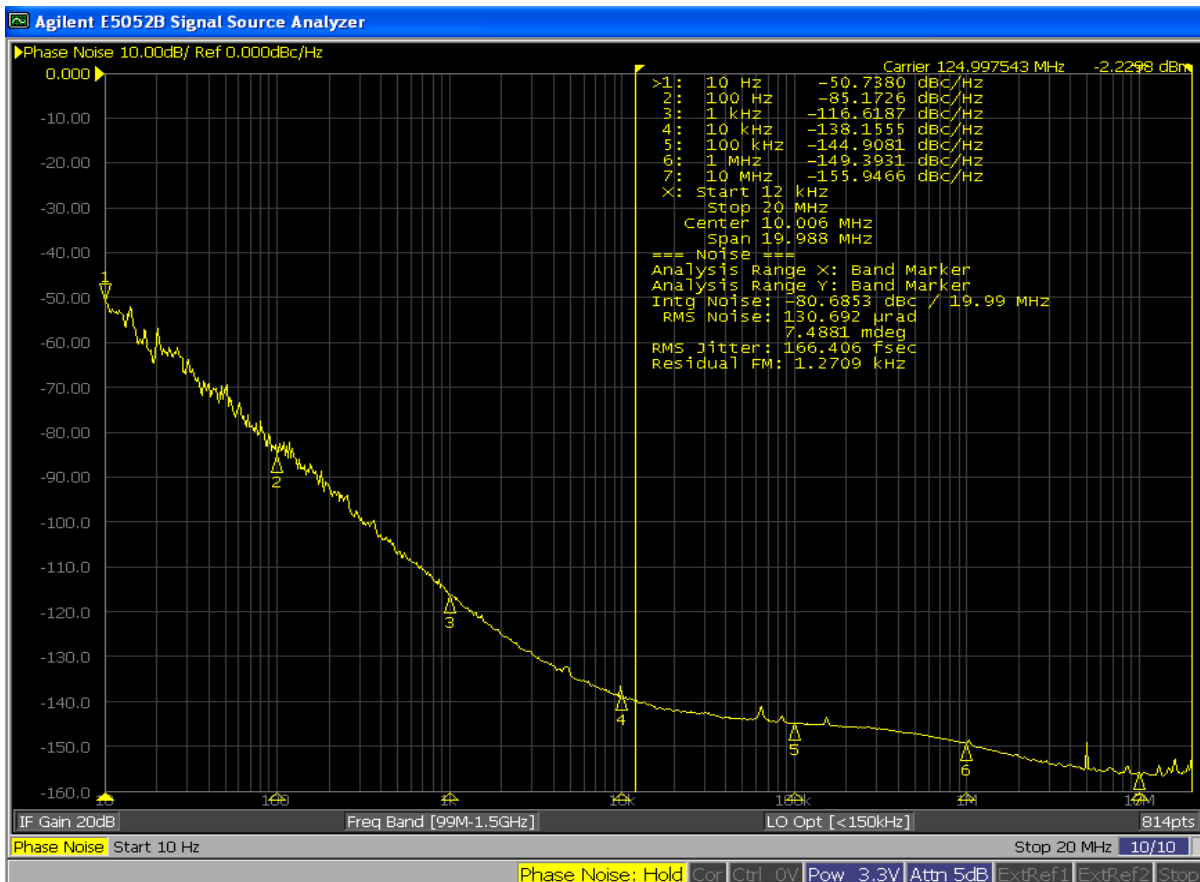


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HPK5761 Package Dimensions and Recommended Solder Pad Layout: unit mm[inches]



Typical Phase Noise Plot 3HPK5761-A-125.000



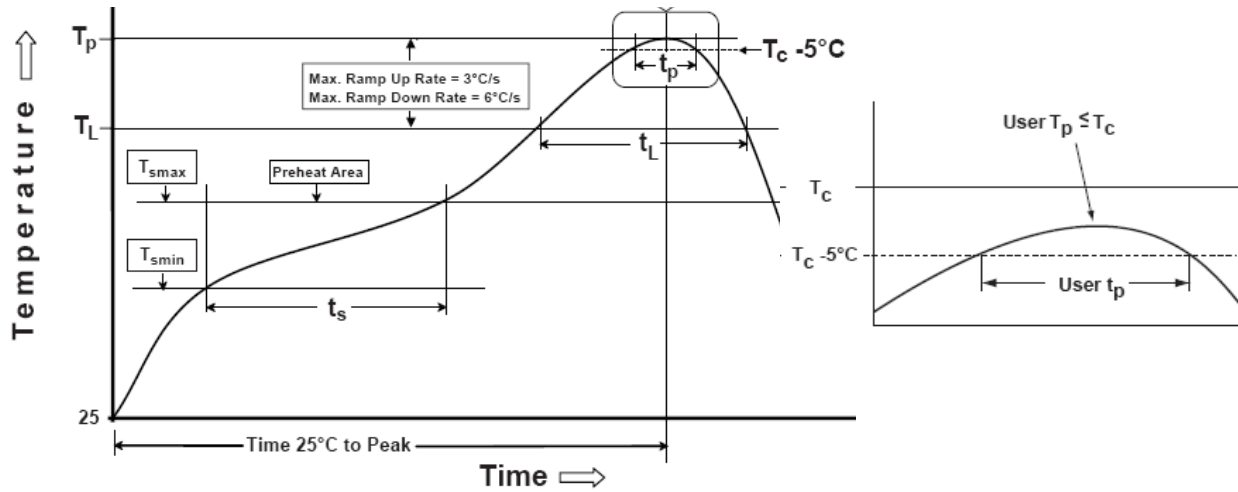
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HPK5761 Recommended Solder Reflow Profile (from IPC/JEDEC J-STD-020D.1)



Profile Feature	Sn-Pb Eutectic Assembly	Pb-free Assembly
Preheat/Soak		
- Temperature min. (Ts min.)	100°C	150°C
- Temperature max. (Ts max.)	150°C	200°C
- Time (ts) (Ts min. to Ts max.)	60 to 120 seconds	60 to 180 seconds
Ramp-up rate (T _L to T _p)	3°C / sec. max.	3°C / sec. max.
Liquidous temperature (T _L)	183°C	217°C
Time (t _L) maintained above T _L	60 to 150 seconds	60 to 150 seconds
Peak package body temperature (T _p)	235°C	260°C
Time (T _p) within 5°C of the classification temperature T _c	10 to 30 seconds	20 to 40 seconds
Ramp-down rate (T _p to T _L)	6°C / second max.	6°C / second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

All temperatures refer to topside of the package, measured on the package body surface.